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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/039,663
Filing Date: October 22, 2001
Appellant(s): EFLAND ET AL.

W. Daniel Swayze, Jr
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/24/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

Appellant's brief includes a statement that claims 1, 2 and 4 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

US 5,973,554	***Yamasaki et al.***	***10-1999***
US 5,468,993	***Tani***	***11-1995***

Wolf et al., Silicon Processing for the VLSI Era, 2000, Lattice Press, volume 1, pages 857-858.

(10) Grounds of Rejection

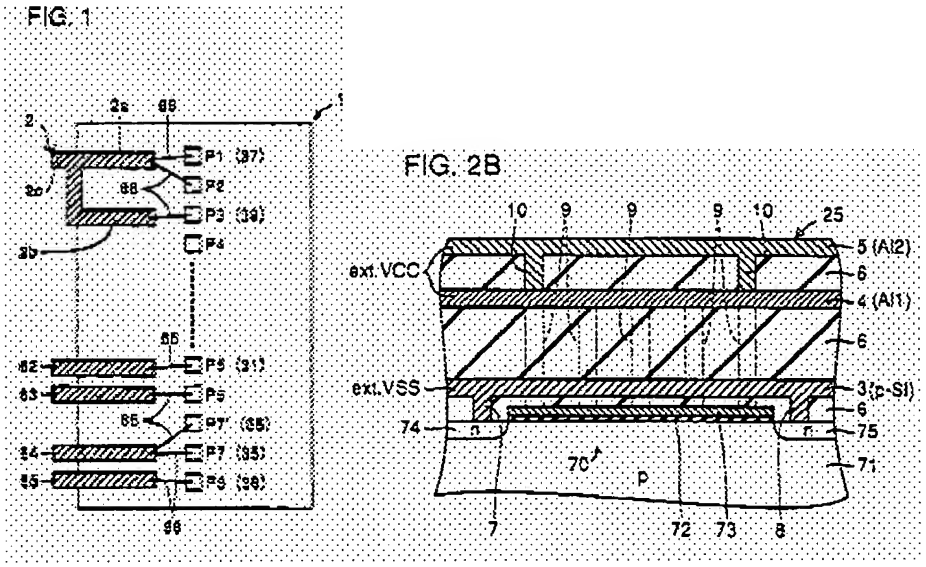
The rejection of claim 2 under 35 U.S.C. 112, second paragraph, has been withdrawn.

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki et al. (US 5,973,554).

Regarding claim 1, Yamasaki (*e.g.* figs. 1-5) shows an integrated circuit chip 71 mounted on a lead frame (61-65) comprising a network distribution lines 5 deposited on the surface of the chip, located directly over active component 70 of the circuit. As shown in figure 5 the lines are conductively and vertically connected to the active components below the lines. Also, the lines are connected to a lead frame 62 by conductors 66 (*e.g.* fig. 1). The majority of the lines patterned as straight lines between the vias and the conductors

respectively, thereby minimizing the distance for power delivery between a selected segment and one or more corresponding active components.



Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554).

Regarding claim 2, Yamasaki shows most aspects of the instant invention, including an integrated circuit having a low interconnection resistance (col. 5/lls. 16-65). Nonetheless, Yamasaki does not disclose that the lines are fabricated with a sheet resistance of less than 1.5 mΩ. The specific sheet resistance claimed by applicant, i.e., 1.5 mΩ, absent any criticality, is only considered to be the "optimum" sheet resistance value of the metal lines disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be

obtained as long as the metal lines are used as already suggested by the Prior Art.

In regards to claim 3, the claim language referring to parasitic electrical losses is considered functional language. Any functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). Moreover, Yamasaki discloses that voltage drop contributes to the device electrical losses (col. 5/lls. 16-65).

Claims 4-5, 7, 8, 11, 15, 20, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993).

Regarding claim 4, Yamasaki (*e.g.* figs. 1-5) discloses a semiconductor device comprising:

- A semiconductor chip having a first and second surfaces;
- An integrated circuit fabricated on the chip first surface having an active components 70;
- A metal layer 4 protected by a mechanically strong, electrically insulating overcoat 6 having a plurality of metal filled vias 9 to make an electrical contact;

- A plurality of windows to expose the circuit contact pads (P1-P5);
- Electrically conductive films 5 deposited on the overcoat and patterned into a network of lines substantially vertically over the active components, the film is in contact with the vias 9 and having an outermost surface being non corrodible and metallurgical attachable metal;
- A lead frame (61-65) having a first plurality of segments providing electrical signal and a second plurality of providing power and ground;
- And electrical conductors 66 connecting the chip contact pads and/or the connecting the network lines with the plurality of segments.

The network pattern distributes the power current and the ground potential (*e.g.* fig. 5). Yamasaki discloses that the chip is mounted on the lead frame. Nonetheless, Yamasaki fails to further specify that the semiconductor chip is mounted on a chip mount pad. Tani discloses that it is conventionally in the art to attach the semiconductor chip to a chip mount pad (col. 1/lls. 17-28). As shown in fig. 3 the second surface of the chip 3 is attached to the chip mount pad 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the second surface of the semiconductor chip to a chip mount pad as it is conventionally in the art as taught by Tani.

Regarding claim 5, Yamasaki discloses that the chip is made of silicon (col. 2/lls. 64-66).

Regarding claim 7, Yamasaki discloses that the circuit comprises multi-layer metallization made of aluminum (col. 8/lls. 9-51).

Regarding claim 8, Yamasaki discloses the claimed invention except for the use of silicon nitride, silicon oxynitride, silicon carbon alloys or polyimide for make the overcoat 6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use of silicon nitride, silicon oxynitride, silicon carbon alloys or polyimide for make the overcoat 6, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ416.

Regarding claim 11, Tani discloses that the semiconductor chip and the bonded portion are sealed by synthetic resin molding or molding (col. 1/lls.19-28). Tani does not specify the process used to make the encapsulation *e.g.* transfer molding process. Nonetheless, this limitation is considered a process limitation. Note that in product related claims only the final product is relevant, not the process of making such as transfer molding. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17. See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has

the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Regarding claim 15, Yamasaki shows that the conductors/ metallurgical attachments are bonding wires.

Regarding claim 20, Yamasaki shows that the conductors are bonding wires.

Regarding claim 21, Tani discloses that the semiconductor chip is bonded to the leads radially disposed around the die pad with gold wires (col. 1/lls.19-28).

Regarding claim 23, Yamasaki shows that the network of lines is electrically connected to the segments that are suitable for outside electrical contact.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Applicant's Admitted Prior Art.

Regarding claim 9, Yamasaki in view of Tani shows most aspects of the instant invention. However, Yamasaki in view of Tani does not disclose that the lead frame is prefabricated from a sheet like material selected from a group consisting of copper, copper alloy, aluminum, iron nickel alloy or invar. However, this limitation is considered to be a process limitation. Note that in product related claims only the final product is relevant, not the process of making such as a pre fabricated lead frame. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17. See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re

Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e). In regards to the material used to make the lead frame, Applicant's Admitted Prior Art discloses that it has been common practice to manufacture single piece lead frames from thin sheets of metal. For reasons of easy manufacturing, the commonly selected starting metals are copper, copper alloy, iron nickel alloys and invar (pg 2/pp. 03). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the lead frame of Yamasaki in view of Tani of copper, copper alloy, iron nickel alloys or invar for easy manufacturing reasons as taught by Applicant's Admitted Prior Art.

Claims 13, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Wolf et al.

Regarding claim 13, Yamasaki in view of Tani shows most aspects of the instant invention including lines and contacts pads attached to the outside part by conductors 66. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, the use of wire bonds or solder balls as connection means is considered an obvious design choice and it is not patentable unless unobvious or unexpected results are obtained from

these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416. For example, the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (see Wolf pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

Regarding claim 20, Yamasaki in view of Tani shows most aspects of the instant invention including bonding wires conductors. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, the use of wire bonding or solder ball connections is considered an obvious design choice and it is not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416. For example, the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the

same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (see Wolf pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

Regarding claim 22, Wolf discloses that the can be made of tin/lead alloy (pages 857-8).

(11) Response to Argument

Applicant's arguments, see appeal brief, filed 5/24/2004, with respect to the rejection(s)of claim(s) 2 under 35 U.S.C. 112 have been fully considered and are persuasive.

Applicant argues that Yamasaki does not disclose an active component. Nonetheless, the device disclosed by Yamasaki includes active components such as MOS transistor (abstract). Applicant argues that the element 70 disclosed by Yamasaki is a capacitor. It is respectfully noted that Yamasaki clearly teaches that the element 70 is a MOS transistor (col. 8/lls. 15-19). MOS transistors are active elements (see attached definition). Yamasaki merely named his MOS transistor "a noise removing capacitor". Nonetheless, a transistor is an active element regardless of how it is named. The fact that Yamasaki is using the capacitance created between the gate of the MOS transistor 70 and the substrate to remove noise (col. 8/lls. 55-65 & fig. 3) does

not change the fact that a MOS transistor by itself is an active device regardless of how Yamasaki chooses to call it.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 07/20/2004 with Mr. Leonardo Andújar (Patent Examiner), Mr. Olik Chaudhuri (Supervisory Patent Examiner), and Nathan J. Flynn (Supervisory Patent Examiner), as the conferees.

Respectfully submitted,

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transient distortion *Electronics.* the distortion of a waveform produced by the inability of a transducer or amplifier to reproduce quick changes in level.

transient error see SOFT ERROR.

transient lunar phenomena *Astronomy.* various mists, reddish glows, flashes of light, and temporary clouds on the moon that a few observers have claimed to see from time to time. Also, LUNAR TRANSIENT PHENOMENA.

transient motion *Physics.* the motion of an object that is suffering the effects of any transients as it approaches its steady-state motion.

transient overshoot *Physics.* the maximum value of a quantity in response to a sudden application of an external agency.

transient phenomena *Electricity.* rapidly changing events that occur in a circuit during a time interval between switch closure and steady-state conditions, or any other temporary events that occur after a change in the circuit or its constants.

transient polymorphism *Genetics.* the temporary presence of two or more allelic variants in a population while one variant is replacing another; an analysis of the gene pool shows only the variants that have

transistance *Electronics.* the basic property of active electronic devices by which they produce gain; transistance makes possible such active devices and circuits as amplifiers, oscillators, bistable circuits, and switching devices.

transistor *Electronics.* **1.** an active semiconductor device, usually made from germanium or silicon and possessing at least three terminals (typically, a base, emitter, and collector); characterized by its ability to amplify current and used in a wide variety of equipment such as amplifiers, oscillators, and switching circuits. **2.** relating to, using, or operated with transistors. Thus, **transistor radio, transistor amplifier,** and so on. (A shortened form of transfer resistor.)

transistor biasing *Electronics.* the process of applying a steady voltage to a transistor, normally between the base and emitter electrodes; the bias voltage determines the operating point of the transistor under quiescent conditions.

transistor characteristics *Electronics.* the parameters that describe the operation of a transistor, such as values of current gain or input resistance and impedance.

transistor chip *Electronics.* a shaped and processed piece of semiconductor material that forms a transistor.

transistor circuit *Electronics.* any electronic circuit employing one or more transistors as the active element(s); found, for example, in amplifiers, oscillators, logic gates, and bistable circuits.

transistor clipping circuit *Electronics.* a circuit that uses transistors to prevent a signal from reaching the peak amplitude it would otherwise attain; this results in a distorted waveform whose peaks appear clipped.

transistor gain *Electronics.* the amplification factor of a transistor amplifier stage; the ratio of signal output voltage or current to signal input voltage or current.

transistor input resistance *Electronics.* the resistance presented by a transistor to the input signal. Also, INPUT RESISTANCE.

transistor magnetic amplifier *Electronics.* a power control circuit consisting of a magnetic amplifier combined with a transistor amplifier; the transistor acts as a preamplifier for the control current to the magnetic amplifier.

transistor-transistor logic *Electronics.* a logic circuit that uses transistors to form the logic elements; circuits are configured as NAND gates, NOR gates, or logic-level inverters. Also, **TTL.**

transit *Transportation Engineering.* the conveyance or transportaion of persons or goods from one place to another, as in public transportation (**mass transit**). *Engineering.* **1.** to rotate a telescope on its horizontal axis 180°, reversing its direction. Also, PLUNGE. **2.** an instrument that is used to determine the passage of a celestial body across a meridian. **3.** an instrument fitted with a telescope that measures vertical and horizontal angles, used in surveying. Also, TRANSIT THEODOLITE. *Astronomy.* **1.** the passage of a celestial body across a meridian or through the field of view of a telescope. **2.** the passage of the planet Mercury or Venus across the sun's disk. **3.** the passage of a moon across the disk of a planet. *Navigation.* a worldwide radio navigation system in which fixes are determined by measuring the Doppler shift of continuous-wave, very ultrahigh-frequency waves transmitted from low-orbit satellites.

Transit *Space Technology.* any of a series of navigation satellites first launched by the U.S. Navy in 1960.

transit bearing *Navigation.* a bearing determined by noting the time at which two features on the earth's surface have the same relative bearing.

transit circle *Engineering.* an astronomical instrument used to measure the zenith distance or the declination of a celestial object. Also, MERIDIAN TRANSIT.

transit declinometer *Engineering.* a surveyor's transit that is used to sight on a mark and determine true direction.

transit instrument see TRANSIT TELESCOPE.

transition *Thermodynamics.* a phase change between the solid, liquid, or gas states. *Quantum Mechanics.* a change of a quantum-mechanical system from one energy state to another. *Telecommunications.* a sequential series of actions that takes place when a process changes from one state to another in response to an input; for example, the change from mark to space or from space to mark. *Molecular Biology.* a mutation in which one purine is substituted for another or one pyrimidine for another in DNA.

transitional fit *Design Engineering.* a fit with varying clearances contingent upon specific tolerance requirements on a shaft or sleeve and hole.

transitional flow *Fluid Mechanics.* a flow in which fluid particles move from a well-behaved laminar pattern into adjacent layers in a random manner that grows in amplitude; the Reynolds stresses are of an order of magnitude equal to the viscous stresses.

transitional frequency *Quantum Mechanics.* the frequency of radiation emitted during a radiative transition.

transition altitude *Aviation.* the altitude at or below which the vertical position of an aircraft is controlled by true altitude. Also, **transition layer.**

transition bands *Materials Science.* in the microstructure of a deformed metal, the boundaries between different regions within a grain that achieve the same imposed strain with a different set of slip systems.

transition element *Chemistry.* in the periodic table, any of a group of elements representing a gradual shift from the strongly electropositive elements of groups IA and IIA to the more electronegative elements of groups IB and IIB; such elements have an atomic structure in which the inner orbitals are systematically filled, providing some unpaired electrons. Also, **transition metal.** *Electromagnetism.* an element or junction that couples one type of transmission system to another, as in the transition from a transmission line to a waveguide.

transition frequency *Acoustical Engineering.* the frequency during a disk recording at which the recording characteristic changes from constant amplitude to constant velocity. Also, CROSSOVER FREQUENCY.

transition function *Computer Technology:* in a sequential machine, the function that determines the next state from the present state and given input, while the output function determines the output.

transition lattice *Metallurgy.* a crystallographic, unstable lattice that forms during solid-state reactions such as eutectoid decomposition.

transition level *Aviation.* the lowest flight level available for use above the transition altitude.

transition loss *Electricity.* a loss at any point in a transmission system; the ratio of the available power from the part of the system ahead of the point under consideration to the power delivered to the part of the system beyond the point under consideration.

transition moment *Quantum Mechanics.* a multipole moment related to the probability of a radiative transition between two states.

transition operators *Artificial Intelligence.* a set of rules that determine all possible next states from a given state of the problem.

transition point *Thermodynamics.* the temperature at which a phase transition takes place. Also, TRANSITION TEMPERATURE. *Aviation.* the point or line in a flow, such as the boundary layer of an airfoil, where laminar flow becomes turbulent. *Electromagnetism.* a point in a circuit along which certain constants change such that there is a reflection of the wave propagating along the circuit.

transition probability *Quantum Mechanics.* the probability per unit time that a particular transition will occur. *Mathematics.* in Markov processes, the fixed (conditional) probability of passing from one state to another.